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Title:

PLL HAVING VCO FOR DIVIDING FREQUENCY

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PLL HAVING VCO FOR DIVIDING FREQUENCY

BACKGROUND

Technical Field

A phase locked loop (abbreviated as "PLL") is disclosed. More specifically, a PLL having a voltage control oscillator (abbreviated as "VCO") configured to divide the frequency outputted from the VCO in wide frequency bands is disclosed.

Description of the Related Art

Fig. 1 is a block diagram illustrating a conventional PLL using a pulse swallow system.

The conventional PLL comprises a phase comparator 1, a low pass filter 2, a VCO 3, a dual modulus prescaler 4, a program counter 5, a swallow counter 6 and a controller 7. The phase comparator 1 compares a reference frequency fr of an external clock signal with a comparison frequency fp of a comparison clock signal PCLK. The VCO 3 generates a clock signal ICLK. The frequency of the clock signal ICLK is proportional to the direct current (DC) signal from the low pass filter 2. The dual modulus prescaler 4 divides a frequency of the clock signal ICLK in the ratios of 1/M and 1/(M+1). The program counter 5 divides a clock signal divided by the prescaler 4 in the ratio of 1/N. The swallow counter 6 divides the clock signal divided by the prescaler 4 in the ratio of 1/A. The controller 7 outputs a mode control signal MC for controlling the prescaler 4 using signals from the program counter 5 and the swallow counter 6.

A frequency fvco of the clock signal ICLK from the VCO 3 is divided by the dual modulus prescaler 4 in the ratios of 1/M and 1/(M+1), and then inputted into the program counter 5 and the swallow counter 6.

The swallow counter 6 is used to control the division ratio of the prescaler 4. The prescaler 4 divides in the ratio of 1/(M+1) until the swallow counter 6 counts A pulses.

After the swallow counter 6 counts A pulses, the prescaler 4 divides in the ratio of 1/M. The comparison frequency fp of the comparison clock signal PCLK is defined by Equation 1.

Equation 1

$$fp = \frac{fvco}{\left\{\left(((M+1)\times N)\times\frac{A}{N}\right)+\left((M\times N)\times\frac{(N-A)}{N}\right)\right\}} = \frac{fvco}{\{((M+1)\times A)+((N-A)\times M)\}}$$

The output frequency fvco of the output clock signal ICLK is defined by Equation 2 (here, fp=fr).

Equation 2

$$\begin{aligned} fvco &= fp\{((M+1)\times A)+((N-A)\times M)\} \\ &= fp(A+M\times N) \\ &= fr(A+M\times N) \end{aligned}$$

In Equation 2, When the value of A varies, the frequency fvco of clock signal ICLK is changed. In this way, if the prescaler 4 is used in the PLL, the channel separation can be the reference frequency fr. Particularly, in a frequency synthesizer of high frequency, a pulse swallow system is used because the prescaler 4 is set in a high division ratio.

Generally, the output frequency fvco of the pulse swallow system is defined by the following equation 3:

Equation 3

$$fvco = \{(M\times N)+A\}\times\frac{fosc}{R}$$

Here, M is the division ratio of the prescaler 24, and N is the value of the program counter 25. A is the value of the swallow counter 26, which is smaller than N. In Equation 3, fosc represents the reference oscillating frequency, and R represents the value of the reference counter.

The VCO of the conventional PLL having a pulse swallow system cannot use various frequency bands due to its non-linear characteristic.

SUMMARY OF THE DISCLOSURE

Accordingly, a PLL having a VCO for dividing frequency that operates linearly in various frequency bands is disclosed.

There is provided a PLL comprising a phase detector, a loop filter and a VCO. The phase detector periodically compares a frequency of an externally inputted

clock signal with that of an internal clock signal, and outputs an output signal resulting from phase difference of the two signals. The loop filter outputs a predetermined voltage in response to a signal from said phase detector. The VCO outputs said internal clock signal having a frequency proportional to said predetermined voltage. Here, the VCO includes a device for adjusting the value of capacitance using an internal control signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating a conventional PLL.

Fig. 2 is a block diagram illustrating a disclosed PLL.

Fig. 3 is a graph illustrating an example of region split and frequency range of a VCO in the PLL of Fig. 2.

Fig. 4 is a circuit diagram illustrating a VCO in the PLL of Fig. 2.

Fig. 5 is a detailed circuit diagram illustrating a capacitor capsule in the VCO of Fig. 4.

Fig. 6 is a graph illustrating tuning characteristics of the VCO of Fig. 4.

Fig. 7 is a graph illustrating output waveform of the VCO of Fig. 4.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

The disclosed PLL will be described in more detail with reference to the accompanied drawings.

Fig. 2 is a block diagram illustrating the disclosed PLL.

The PLL comprises a phase comparator 11, a low pass filter 12, a VCO 13, a dual modulus prescaler 14, a program counter 15, a swallow counter 16, a controller 17 and a control bit generator 18. The phase comparator 11 compares a reference frequency fr of an external clock signal ECLK with a comparison frequency fp of a comparison clock signal PCLK. The VCO 13 generates an internal clock signal ICLK of frequency proportional to a DC signal of the low pass filter 12. The dual modulus prescaler 14 divides an internal clock signal ICLK in the ratios of 1/M and 1/(M+1). The program counter 15 divides a clock signal from the prescaler 14 in the ratio of 1/N. The swallow counter 16 divides a clock signal from the prescaler 14 in the ratio of 1/A. The controller 17 controls the prescaler 14 by using output signals from

the program counter 15 and the swallow counter 16. The control signal generator 18 generates a control signal CB<0:4> for controlling the VCO 13.

An output frequency fvco of the internal clock signal ICLK is divided by the dual modulus prescaler 34 in the ratios of 1/M and 1/(M+1). The divided frequency is inputted into the program counter 15 and the swallow counter 16.

The swallow counter 16 is used to control the division ratio of the prescaler 14. The prescaler 14 divides in the ratio of 1/(M+1) until the swallow counter 16 counts A pulses.

After the swallow counter 16 counts A pulses, the prescaler 15 divides in the ratio of 1/M.

The disclosed PLL uses the values of N and A in order to control the VCO 13. That is, the control signal generator 18 generates a control signal for controlling the VCO 13 by using the values of N and A.

Accordingly, a method should be considered to satisfy the whole range of frequency in a given variable voltage range and to reduce the actual oscillating frequency Kvco by using an oscillating frequency division method.

Fig. 3 is a graph illustrating an example for dividing the frequency range GSM of the VCO 13in the PLL of Fig. 2.

Referring to Fig. 3, if the range of variable voltage is 1V in the frequency range of GSM from 1150MHz to 1230MHz, the oscillating frequency Kvco generally has the value of 80MHz/V.

However, the whole frequency range can be satisfied by fixing the frequency range at 10MHz and selecting a partial area of each frequency using an external auxiliary circuit. Each oscillating frequency Kvco can have a small value of 10MHz/V.

In the disclosed PLL, the frequency division VCO 13 is used to have good characteristics in the wide range of frequency. When the output frequency fvco from the VCO 13 reaches its corresponding frequency area nearby, the disclosed PLL selects a corresponding section.

If a voltage gain of the VCO 33 is determined, for example, as 10MHz/V, the number of the VCO 33 can be determined. As a result, the control signal generator 18 generates the control signal CB.

Fig. 4 is a circuit diagram illustrating the VCO of the PLL of Fig. 2.

The VCO 13 comprises a constant current source 21, PMOS transistors PM1 and PM2, a capacitor capsule 22, an inductor L, one-way capacitors OC1 and OC2, and NMOS transistors NM1 and NM2. The PMOS transistors PM1 and PM2 are cross-coupled. The capacitor capsule 22 is connected between output terminals OUTP and OUTN. The inductor L is connected between the output terminals OUTP and OUTN. The one-way capacitor OC1 is connected between the output terminal OUTP and an input terminal Vc, and the one-way capacitor OC2 is connected between the input terminal Vc and the output terminal OUTN. The NMOS transistors NM1 and NM2 are cross-coupled. Here, the capacitor capsule 22 includes a capacitor array for selecting a section.

Fig. 5 is a detailed circuit diagram illustrating the capacitor capsule 22 in the VCO 13 of Fig. 4.

The capacitor capsule 22 comprises a capacitor C1 having one terminal connected to a pair of switches NM3 and NM4 and the other terminal connected to a pair of switches NM5 and NM6. The switches NM3 and NM4 are connected between the one terminal of the capacitor C1 and the output terminal OUTP. The switches NM5 and NM6 are connected between the other terminal of the capacitor C1 and the output terminal OUTN. Here, capacitors C2~C6 are connected in parallel between the switch NM3 and the output terminal OUTP by the switches NM7~NM11, and capacitors C7~C11 are connected in parallel between switch NM5 and the output terminal OUTN by the switches NM7~NM16.

Although the switches NM3~NM16 formed of NMOS transistors are exemplified herein, various types of switches can be used according to systems.

Each switch NM3~NM16 is controlled by the control signal CB<0:4> outputted from the control signal generator 18.

As a result, the oscillating frequency can be varied by changing capacitance of the capacitor capsule 22 by adjusting the control signal CB<0:4>.

Fig. 6 is a graph illustrating tuning characteristics of the VCO 13 of Fig. 4.

Referring to Fig. 6, each oscillating frequency waveform linearly decreased depending on tuning voltage, and overlapped with the neighboring waveform.

In general, the frequency hops according to systems using the VCO. As shown in Fig. 7, the capacitance to the frequency hopping is compensated by the

capacitor C1, which is inserted in parallel, by using the switches NM3~NM6 and controlled by the control signal CB<0:1>. Since the RF1 capsule has different ratio to each capacitor C1, a weighted circuit having proper weighting is required through simulation.

Fig. 7 is a graph illustrating output waveform of the VCO of Fig. 4.

Referring to Fig. 7, different frequencies are shown depending on each control signal CB<0:4>. Peak voltages of the output signals change depending on frequencies.

As a result, an additional frequency compensating signal is not required because the frequencies may be automatically pre-compensated by a control signal used in a PLL.

In conventional PLLs, there are installed external components such as a VCO or a filter outside of the PLLs, which influence on cost and yield of the product.

However, the disclosed PLL having a VCO therein can be configured into a single chip.

As a result, frequencies may be automatically pre-compensated in the disclosed PLL, thereby simplifying the embodiment of the whole PLL and enabling accurate compensation.

As discussed earlier, since frequencies may be automatically pre-compensated by control signals used in the PLL, additional frequency compensation signals are not required. Additionally, the disclosed PLL having a VCO therein can be configured into a single chip.

While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and described in detail herein. However, it should be understood that the invention is not limited to the particular forms disclosed. Rather, the invention covers all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined in the appended claims.